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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,492	10/30/2001	Dominic Paulraj	03226/076001; P5661	1317

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,492	PAULRAJ, DOMINIC	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *July 21, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are presented for examination.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilson.

6. Wilson teaches the invention (claim 1) as claimed including a reconfigurable cache memory comprising:

a programmable memory unit using programmable logic (e.g., see paragraph 0036);

a functional unit in communication with the programmable memory unit, wherein the functional unit executes applications using the programmable memory unit (e.g., see Figure 14); and,

reconfiguration module for determining an optimal configuration of memory for a particular application and programming the programmable memory unit to the optimal configuration as the ability to reconfigure FPGA (field-programmable gate array) devices in the field (e.g., see paragraphs 0050-0051).

As to claim 2, Wilson teaches the programmable memory unit is a field-programmable gate array (e.g., see paragraphs 0050-0051).

As to claim 3, Wilson teaches the reconfiguration module supplies a vector representing the optimal configuration determined to the programmable memory unit as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204).

As to claim 4, Wilson teaches the reconfiguration module determines the optimal configuration by collecting performance information and analyzing the collected performance information as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204).

As to claim 5, Wilson teaches the programmable memory unit, the functional unit, and the reconfiguration unit are combined into a single system as the hardware/software codesign (e.g., see paragraphs 0196-0229).

7. Wilson teaches the invention (claim 6) as claimed including a method of reconfiguring cache memory comprising:

determining an optimal configuration of memory for a particular application executed by a functional unit using a programmable memory unit as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204); and,

programming the programmable memory unit to the optimal configuration (e.g., see paragraphs 0197-0204).

As to claim 7, Wilson teaches determining another optimal configuration of memory for another particular application executed by the functional unit using the programmable memory unit and programming the programmable memory unit to another optimal configuration as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204) and as the ability of the system to reconfigure the memory in the field (e.g., see paragraph 0050-0051).

As to claim 8, Wilson teaches dynamically switching between programming the programmable memory unit to the optimal configuration and another optimal configuration based on which application is being executed by the functional unit as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0229).

As to claim 9, Wilson teaches the determining of the optimal configuration of memory for a particular application executed by a functional unit using a programmable memory unit comprises:

collecting performance information and analyzing the collected performance information (e.g., see paragraphs 0197-0204).

As to claim 10, Wilson teaches the programming of the programmable memory unit comprises:

creating a vector representing the optimal configuration and sending the vector to the programmable memory unit as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204).

As to claim 11, Wilson teaches a field programmable gate array configuration generator tool creates the vector as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204).

As to claim 13, Wilson teaches a means for determining another configuration of memory for another particular application executed by the functional unit using the programmable memory unit and a means for programming the programmable memory unit to another optimal configuration as the hardware/software codesign (e.g., see paragraphs 0196-0229) and as the ability of the system to reconfigure the memory in the field (e.g., see paragraph 0050-0051) .

As to claim 14, Wilson teaches a means for dynamically switching between programming the programmable memory unit to the optimal configuration and the another optimal configuration based on which application is being executed by the functional unit as the hardware/software codesign (e.g., see paragraphs 0196-0229).

As to claim 15, Wilson teaches the means for determining of the optimal configuration of memory for a particular application executed by a functional unit using a programmable memory unit comprises means for collecting and analyzing performance information as the hardware/software codesign (e.g., see paragraphs 0196-0229).

As to claim 16, Wilson teaches the means for programming of the programmable memory unit comprises a means for creating a vector representing the optimal configuration and

sending the vector to the programmable memory unit as the hardware/software codesign (e.g., see paragraphs 0196-0229).

8. Wilson teaches the invention (claim 17) as claimed including a reconfigurable cache comprising:

a field-programmable gate array (e.g., see paragraph 0036 and 0050-0051);

a functional unit in communication with the field-programmable gate array, wherein the functional unit executes applications using the field-programmable gate array as the hardware/software codesign (e.g., see paragraphs 0196-0229);

reconfiguration module for determining an optimal configuration of memory for a particular application and programming the field-programmable gate array to the optimal configuration as the hardware/software codesign (e.g., see paragraphs 0196-0229); and,

wherein the reconfiguration module determines the optimal configuration by collecting performance information and analyzing the collected performance information as the hardware/software codesign (e.g., see paragraphs 0196-0229).

As to claim 18, Wilson teaches the reconfiguration module supplies a vector representing the optimal configuration determined to the field programmable gate array as the hardware/software codesign (e.g., see paragraphs 0196-0229).

As to claim 19, Wilson teaches the field programmable gate array, the functional unit, and the reconfiguration unit are combined into a single system as the hardware/software codesign (e.g., see paragraphs 0196-0229).

9. Wilson teaches the invention (claim 12) as claimed including a reconfigurable cache memory comprising:

means for determining an optimal configuration of memory for a particular application executed by a functional unit using a programmable memory unit as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204); and,

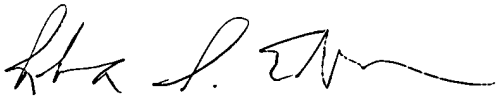
means for programming the programmable memory unit to the optimal configuration as the system codesign using algorithms to optimize the characteristics of the hardware and software (e.g., see paragraphs 0197-0204).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.



Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

November 28, 2004